

SW8N70K-VB TO252 Datasheet

N-Channel 700V(D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10\text{ V}$	0.45
Q_g max. (nC)	70	
Q_{gs} (nC)	9	
Q_{gd} (nC)	16	
Configuration	Single	

FEATURES

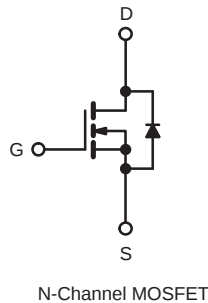
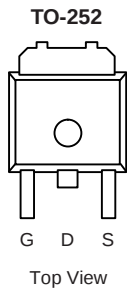
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	700	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	11	A
		T _C = 100 °C		8	
Pulsed Drain Current ^a			I _{DM}	28	
Linear Derating Factor				1.4	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	226	mJ
Maximum Power Dissipation			P _D	156	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T _J = 125 °C		dV/dt	37	V/ns
Reverse Diode dV/dt ^d		28			
Soldering Recommendations (Peak Temperature) ^c	for 10 s			300	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
 b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 4\text{ A}$.
 c. 1.6 mm from case.
 d. $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ }^\circ\text{C}$.

THERMAL RESISTANCE RATINGS

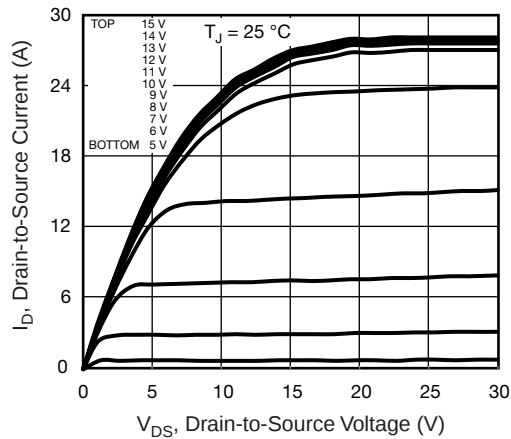
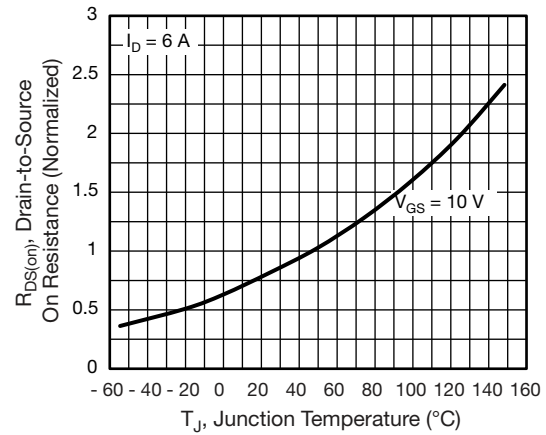
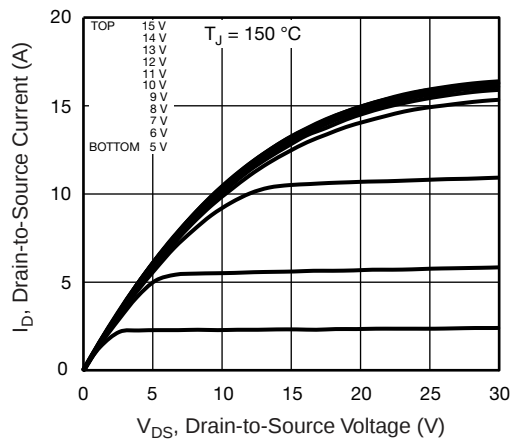
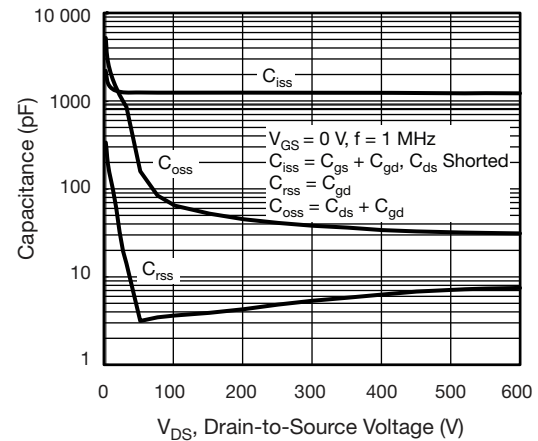
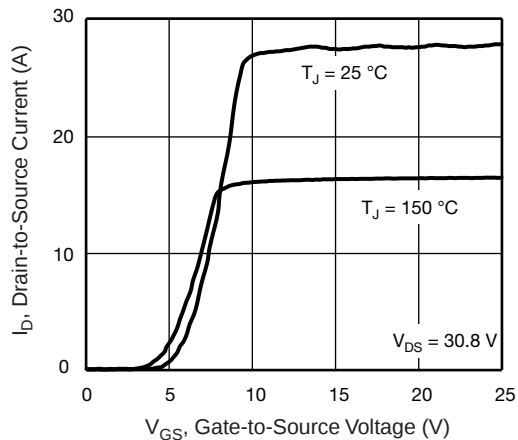
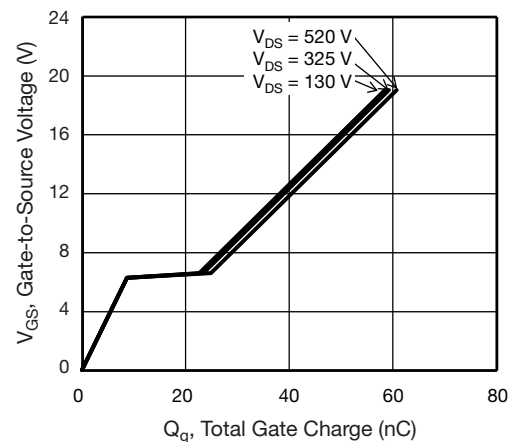
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

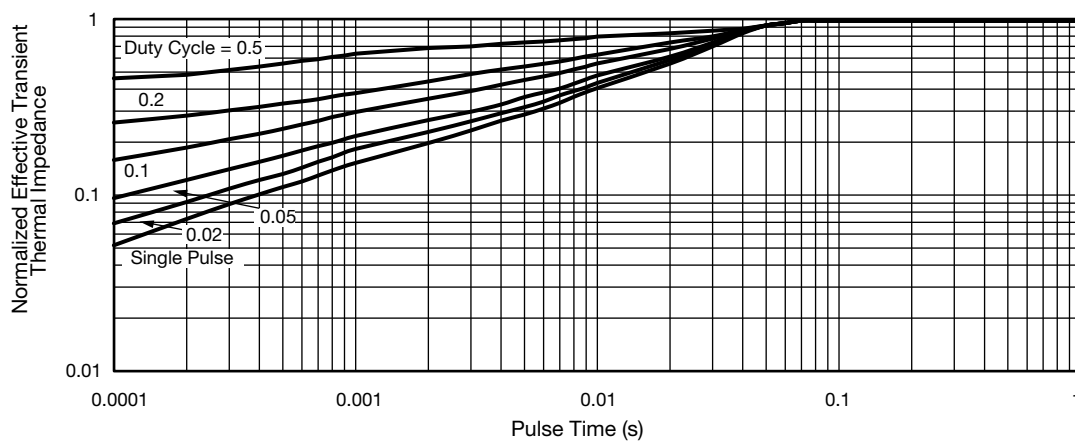
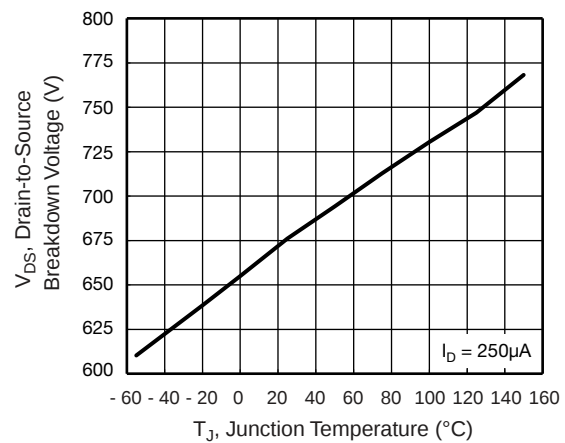
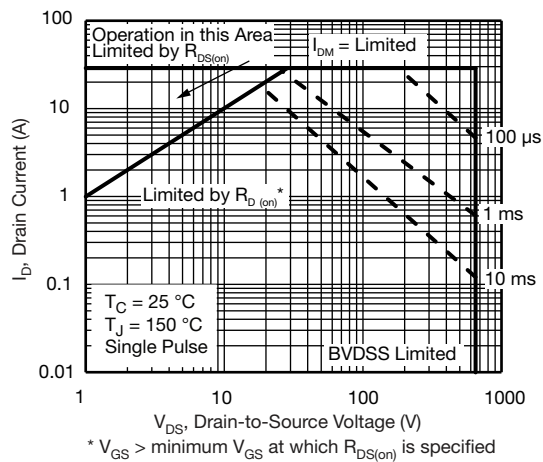
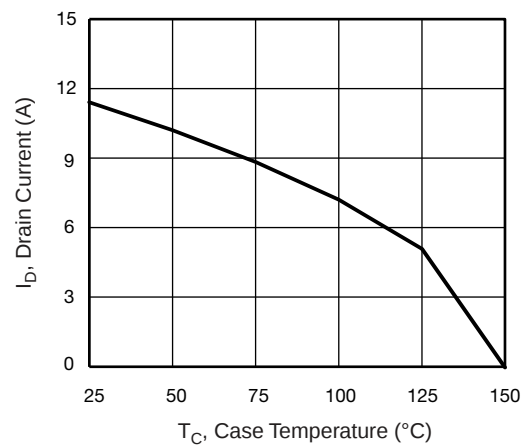
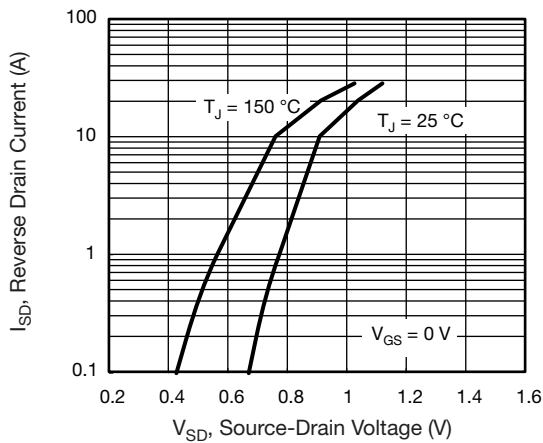
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		700	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.78	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 700 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6 A	-	0.45	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 6 A		-	3.5	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	1224	-	pF
Output Capacitance	C _{oss}			-	65	-	
Reverse Transfer Capacitance	C _{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	50	-	pF
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	160	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6 A, V _{DS} = 520 V	-	35	70	nC
Gate-Source Charge	Q _{gs}			-	9	-	
Gate-Drain Charge	Q _{gd}			-	16	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 520 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	16	32	ns
Rise Time	t _r			-	19	38	
Turn-Off Delay Time	t _{d(off)}			-	35	70	
Fall Time	t _f			-	18	36	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.81	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	11	A
Pulsed Diode Forward Current	I _{SM}			-	-	28	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 6 A, V _{GS} = 0 V		-	1.0	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 6 A, dI/dt = 100 A/μs, V _R = 25 V		-	309	618	ns
Reverse Recovery Charge	Q _{rr}			-	3.8	7.6	μC
Reverse Recovery Current	I _{RRM}			-	21	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



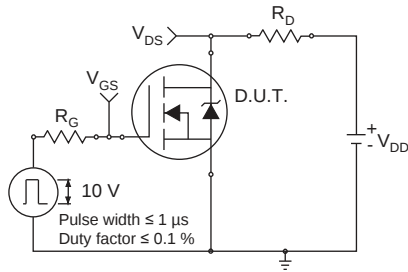


Fig. 12 - Switching Time Test Circuit

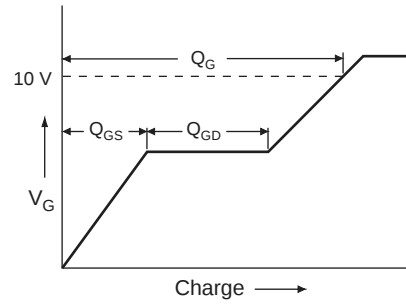


Fig. 16 - Basic Gate Charge Waveform

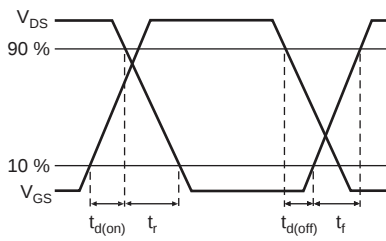


Fig. 13 - Switching Time Waveforms

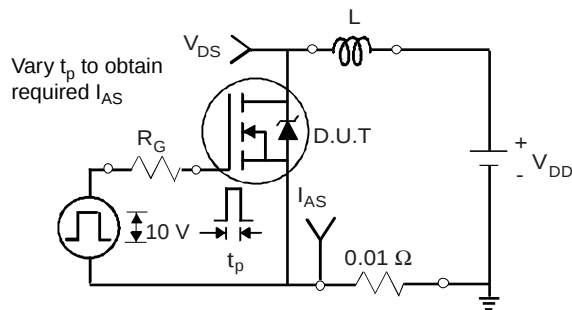


Fig. 14 - Unclamped Inductive Test Circuit

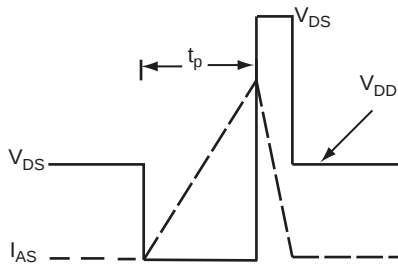


Fig. 15 - Unclamped Inductive Waveforms

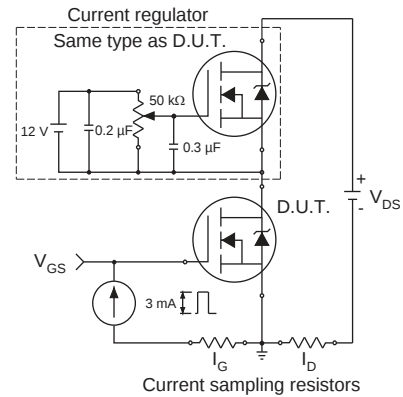
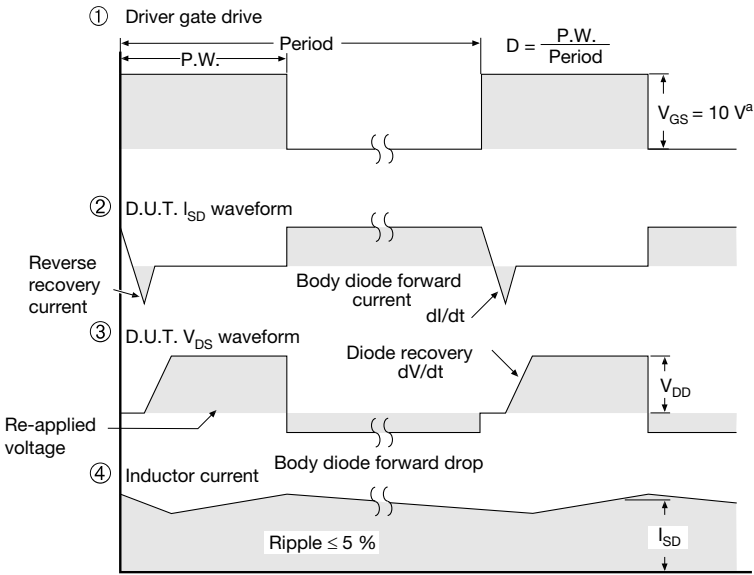
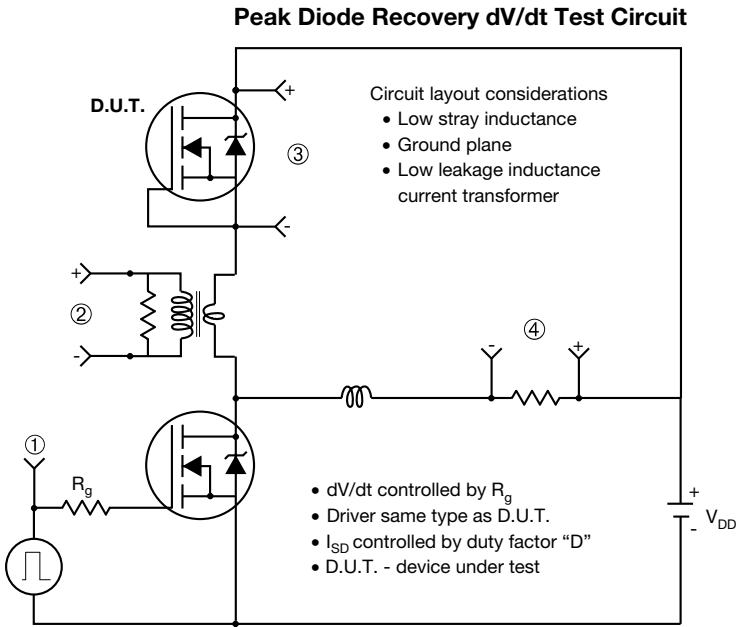


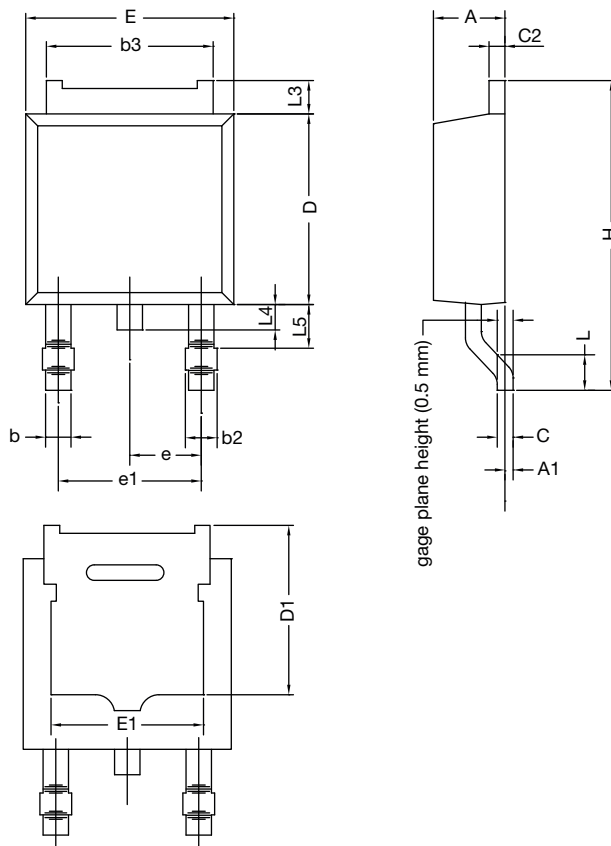
Fig. 17 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

TO-252AA CASE OUTLINE

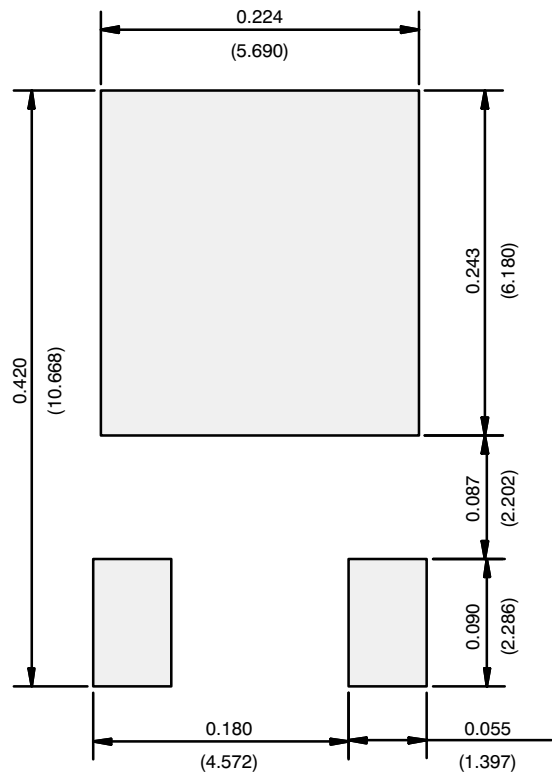


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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